

# TLE 6258-2

## LIN Transceiver

Automotive Power



Never stop thinking.

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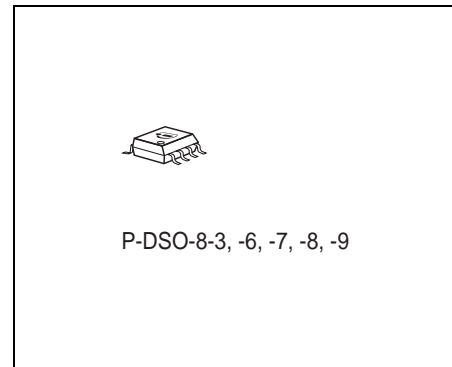
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**Features**

- Single-wire transceiver, suitable for **LIN** protocol
- Compatible to LIN specification 1.2, 1.3 and 2.0
- Compatible to ISO 9141 functions
- Transmission rate up to 20 kBaud
- Very low current consumption in stand-by mode
- Wake-up from Bus
- Short circuit proof to ground and battery
- Overtemperature protection



**Description**

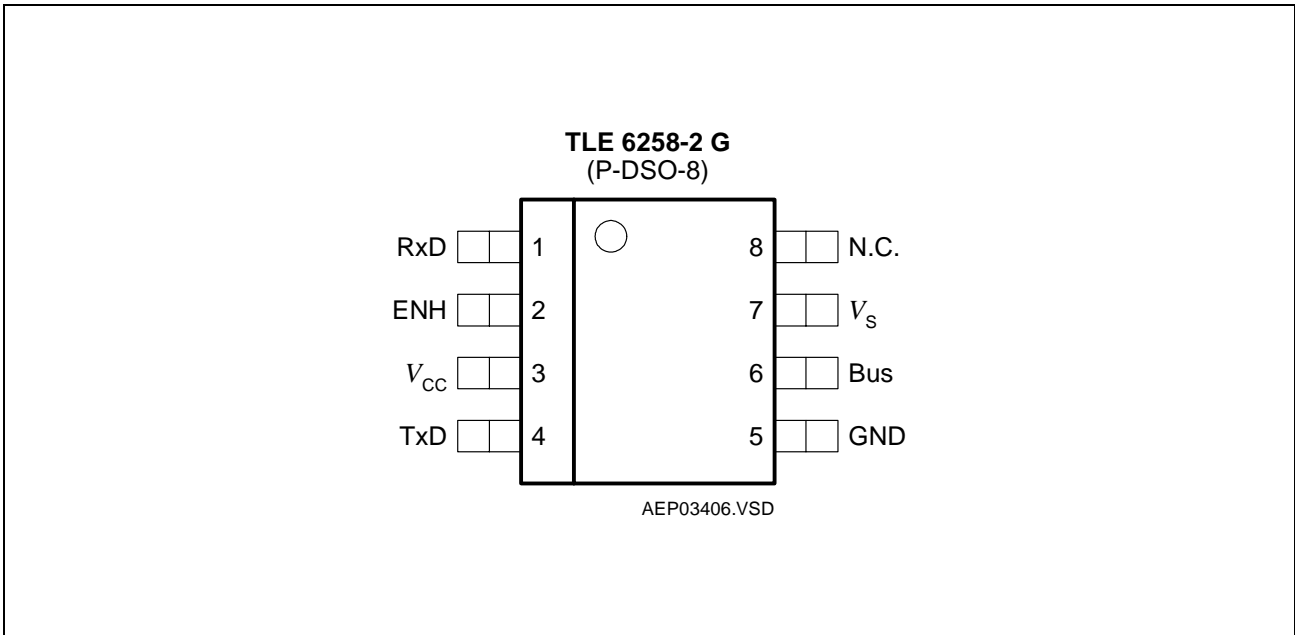
The single wire transceiver TLE 6258-2 is a monolithic integrated circuit in a P-DSO-8-3 package. It works as an interface between the protocol controller and the physical bus. The TLE 6258-2 is especially suitable to drive the bus line in LIN systems in automotive and industrial applications. Further it can be used in standard ISO9141 systems.

In order to reduce the current consumption the TLE 6258-2 offers a stand-by mode. A wake-up caused by a message on the bus sets the RxD output low until the device is switched to normal operation mode.

The IC is based on the Smart Power Technology SPT<sup>®</sup> which allows bipolar and CMOS control circuitry in accordance with DMOS power devices existing on the same monolithic circuit.

The TLE 6258-2 is designed to withstand the severe conditions of automotive applications.

Type	Ordering Code	Package
TLE 6258-2 G	Q67006-A9695	P-DSO-8-3



**Figure 1** Pin Configuration (top view)

**Table 1** Pin Definitions and Functions

Pin No.	Symbol	Function
1	RxD	<b>Receive data output</b> ; integrated pull-up, LOW in dominant state
2	ENN	<b>Enable not input</b> ; integrated 30 kΩ pull-up, transceiver in normal operation mode when LOW
3	V <sub>CC</sub>	<b>5 V supply input</b>
4	TxD	<b>Transmit data input</b> ; integrated pull-up, LOW in dominant state
5	GND	<b>Ground</b>
6	Bus	<b>Bus output/input</b> ; internal 30 kΩ pull-up, LOW in dominant state
7	V <sub>S</sub>	<b>Battery supply input</b>
8	n.c.	<b>Not connected</b>

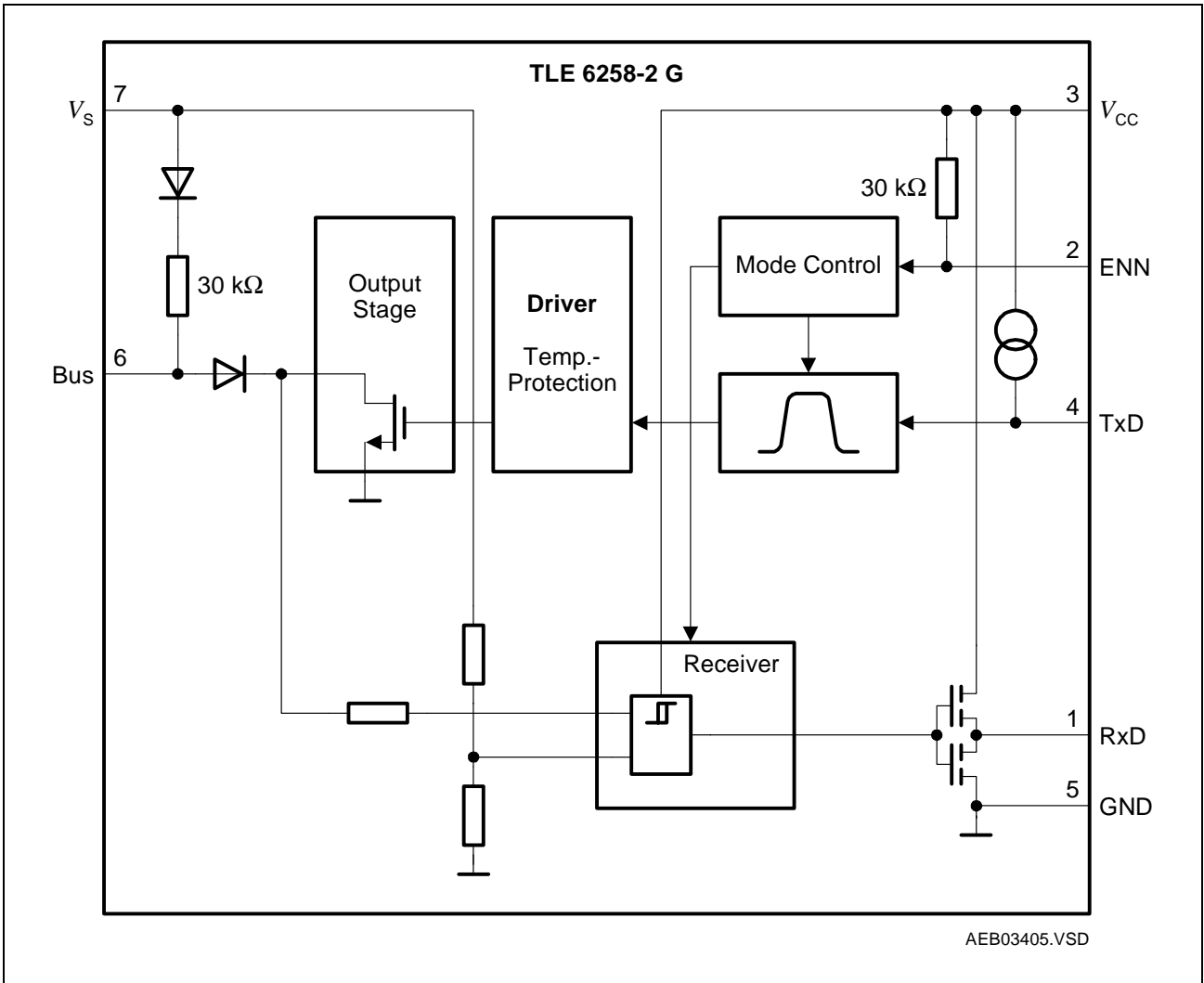
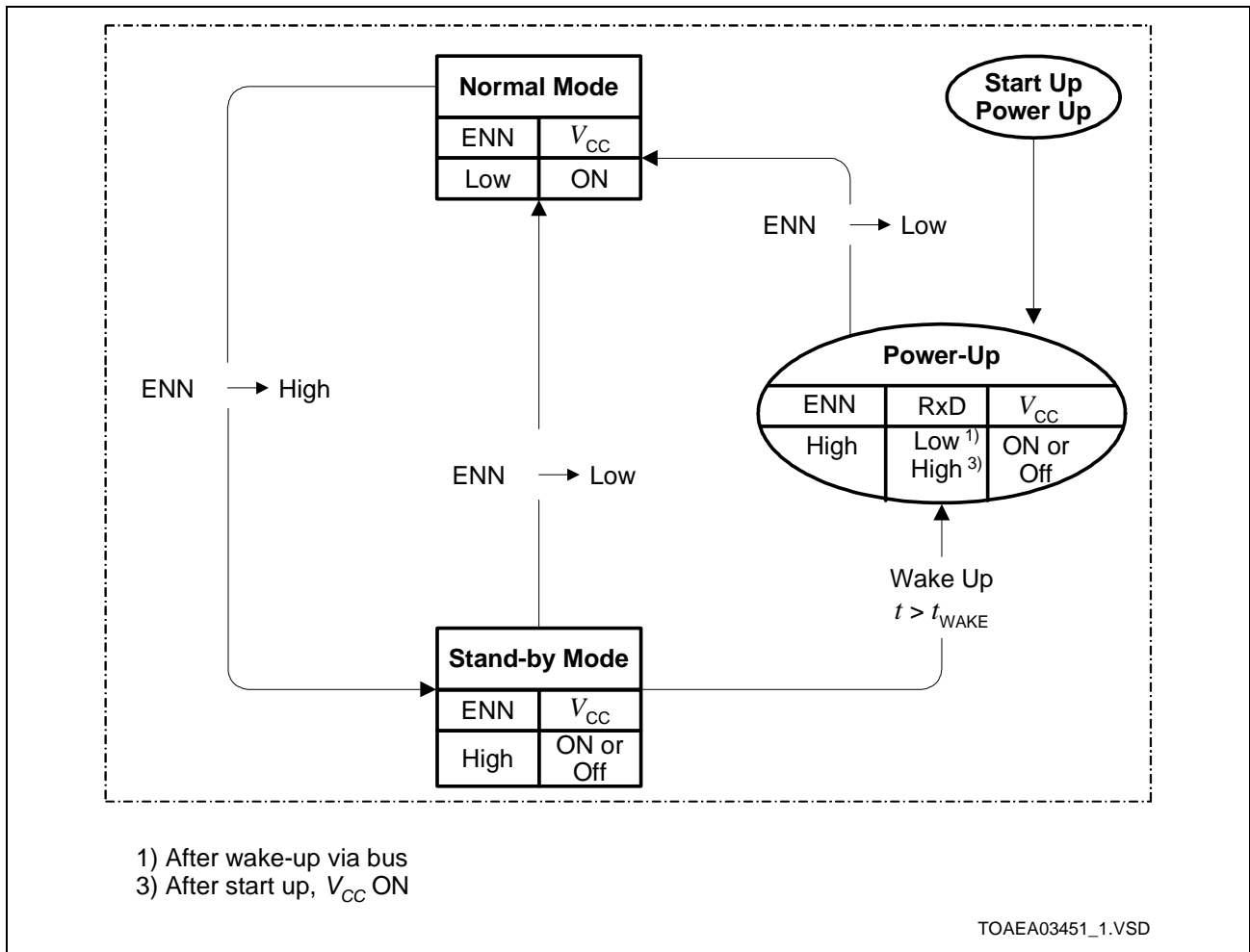


Figure 2 Functional Block Diagram

### Application Information



**Figure 3 State Diagram**

For fail safe reasons the TLE 6258-2 has already a pull-up resistor of 30 kΩ implemented. To achieve the required timings for the dominant to recessive transition of the bus signal an additional external termination resistor of 1 kΩ is required. It is recommended to place this resistor in the master node. To avoid reverse currents from the bus line into the battery supply line in case of an unpowered node, it is recommended to place a diode in series to the external pull-up. For small systems (low bus capacitance) the EMC performance of the system is supported by an additional capacitor of at least 1 nF in the master node (see [Figure 6](#)).

In order to reduce the current consumption the TLE 6258-2 offers a stand-by mode. This mode is selected by switching the Enable Not (ENN) input high (see [Figure 3](#)). In the stand-by mode a wake-up caused by a message on the bus is indicated by setting the RxD output low. When entering the normal mode this wake-up flag is reset and the RxD output is released to transmit the bus data.

**Table 2 Absolute Maximum Ratings**

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
<b>Voltages</b>					
Supply voltage	$V_{CC}$	-0.3	6	V	–
Battery supply voltage	$V_S$	-0.3	40	V	–
Bus input voltage	$V_{bus}$	-20	32	V	–
Bus input voltage	$V_{bus}$	-20	40	V	$t < 1\text{ s}$
Logic voltages at EN, TxD, RxD	$V_I$	-0.3	$V_{CC} + 0.3$	V	$0\text{ V} < V_{CC} < 5.5\text{ V}$
Electrostatic discharge voltage at $V_S$ , Bus	$V_{ESD}$	-4	4	kV	human body model (100 pF via 1.5 kΩ)
Electrostatic discharge voltage	$V_{ESD}$	-2	2	kV	human body model (100 pF via 1.5 kΩ)
<b>Temperatures</b>					
Junction temperature	$T_j$	-40	150	°C	–

*Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit*

**Table 3 Operating Range**

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
Supply voltage	$V_{CC}$	4.5	5.5	V	–
Battery Supply Voltage	$V_S$	6	35	V	–
Junction temperature	$T_j$	-40	150	°C	–
<b>Thermal Shutdown (junction temperature)</b>					
Thermal shutdown temp.	$T_{jSD}$	150	170	190	°C
Thermal shutdown hyst.	$\Delta T$	–	10	–	K
<b>Thermal Resistances</b>					
Junction ambient	$R_{thj-a}$	–	185	K/W	–

**Table 4 Electrical Characteristics**

4.5 V <  $V_{CC}$  < 5.5 V; 6.0 V <  $V_S$  < 27 V;  $R_L = 500 \Omega$ ;  $V_{ENN} < V_{ENN,ON}$ ;  $-40 \text{ }^\circ\text{C} < T_j < 125 \text{ }^\circ\text{C}$ ; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Remark
		Min.	Typ.	Max.		
<b>Current Consumption</b>						
Current consumption	$I_{CC}$	–	0.4	0.7	mA	recessive state; $V_{TxD} = V_{CC}$
Current consumption	$I_S$	–	0.5	1.0	mA	recessive state; $V_{TxD} = V_{CC}$
Current consumption	$I_{CC}$	–	0.4	0.8	mA	dominant state; $V_{TxD} = 0 \text{ V}$ ; without $R_L$
Current consumption	$I_S$	–	1.3	2.0	mA	dominant state; $V_{TxD} = 0 \text{ V}$ ; without $R_L$
Current consumption	$I_{CC}$		0.4	0.7	mA	power-up mode
Current consumption	$I_S$	–	0.5	1.0	mA	power-up mode, $V_{CC} = 0 \text{ V}$ , $V_S = 13.5 \text{ V}$
Current consumption	$I_{CC}$	1	3	10	$\mu\text{A}$	stand-by mode
Current consumption	$I_S$	–	18	40	$\mu\text{A}$	stand-by mode



**Table 4 Electrical Characteristics (cont'd)**

4.5 V <  $V_{CC}$  < 5.5 V; 6.0 V <  $V_S$  < 27 V;  $R_L = 500 \Omega$ ;  $V_{ENN} < V_{ENN,ON}$ ; -40 °C <  $T_j$  < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Remark
		Min.	Typ.	Max.		
<b>Enable Not Input (pin ENN)</b>						
HIGH level input voltage threshold	$V_{ENN,off}$	–	2.8	$0.7 \times V_{CC}$	V	low power mode
LOW level input voltage threshold	$V_{ENN,on}$	$0.3 \times V_{CC}$	2.2	–	V	normal operation mode
ENN input hysteresis	$V_{ENN,hys}$	300	600	900	mV	–
ENN pull-up resistance	$R_{ENN}$	15	30	60	k $\Omega$	–
<b>Receiver Output RxD</b>						
HIGH level output current	$I_{RD,H}$	-1.2	-0.8	-0.5	mA	$V_{RD} = 0.8 \times V_{CC}$
LOW level output current	$I_{RD,L}$	0.5	0.8	1.2	mA	$V_{RD} = 0.2 \times V_{CC}$
<b>Transmission Input TxD</b>						
HIGH level input voltage threshold	$V_{TD,H}$	–	2.9	$0.7 \times V_{CC}$	V	recessive state
TxD input hysteresis	$V_{TD,hys}$	300	700	900	mV	–
LOW level input voltage threshold	$V_{TD,L}$	$0.3 \times V_{CC}$	2.1	–	V	dominant state
TxD pull-up current	$I_{TD}$	-150	-110	-70	$\mu$ A	$V_{TxD} < 0.3 \times V_{CC}$

**Table 4 Electrical Characteristics (cont'd)**

4.5 V <  $V_{CC}$  < 5.5 V; 6.0 V <  $V_S$  < 27 V;  $R_L = 500 \Omega$ ;  $V_{ENN} < V_{ENN,ON}$ ; -40 °C <  $T_j$  < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Remark
		Min.	Typ.	Max.		
<b>Bus Receiver</b>						
Receiver threshold voltage, recessive to dominant edge	$V_{bus,rd}$	0.44 $\times V_S$	0.48 $\times V_S$	–	V	$-8 \text{ V} < V_{bus} < V_{bus,dom}$
Receiver threshold voltage, dominant to recessive edge	$V_{bus,dr}$	–	0.56 $\times V_S$	$0.6 \times V_S$	V	$V_{bus,rec} < V_{bus} < 20 \text{ V}$
Receiver hysteresis	$V_{bus,hys}$	0.02 $\times V_S$	0.04 $\times V_S$	$0.1 \times V_S$	mV	$V_{bus,hys} = V_{bus,rec} - V_{bus,dom}$
Receiver threshold center voltage	$V_{bus,cnt}$	0.475 $\times V_S$	$0.5 \times V_S$	0.525 $\times V_S$		LIN2.0 table 3.1
Input leakage current	$I_{bus,lek}$	-1			mA	$V_{bus} = 0 \text{ V}$ , $V_{bat} = 12 \text{ V}$ , pull-up resistor as specified in LIN2.0
Wake-up threshold voltage	$V_{wake}$	0.40 $\times V_S$	$0.5 \times V_S$	$0.6 \times V_S$	V	–
<b>Bus Transmitter</b>						
Bus recessive output voltage	$V_{bus,rec}$	$0.9 \times V_S$	–	$V_S$	V	$V_{TxD} = V_{CC}$
Bus dominant output voltage	$V_{bus,dom}$	0	–	2	V	$V_{TxD} = 0 \text{ V}$ $7.3 \text{ V} < V_S < 27 \text{ V}$
		0	–	1.2	V	$V_{TxD} = 0 \text{ V}$ $6 \text{ V} < V_S < 7.3 \text{ V}$
Bus short circuit current	$I_{bus,sc}$	40	100	150	mA	$V_{bus,short} = 13.5 \text{ V}$
Leakage current	$I_{bus,lk}$	-1	-	–	mA	$V_{CC} = 0 \text{ V}$ , $V_S = 0 \text{ V}$ , $V_{bus} = -8 \text{ V}$ ,
		–	10	20	$\mu\text{A}$	$V_{CC} = 0 \text{ V}$ , $V_S = 13.5 \text{ V}$ , $V_{bus} = 20 \text{ V}$ ,
Bus pull-up resistance	$R_{bus}$	20	30	47	k $\Omega$	–

**Table 4 Electrical Characteristics (cont'd)**

4.5 V < V<sub>CC</sub> < 5.5 V; 6.0 V < V<sub>S</sub> < 27 V; R<sub>L</sub> = 500 Ω; V<sub>ENN</sub> < V<sub>ENN,ON</sub>; -40 °C < T<sub>j</sub> < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

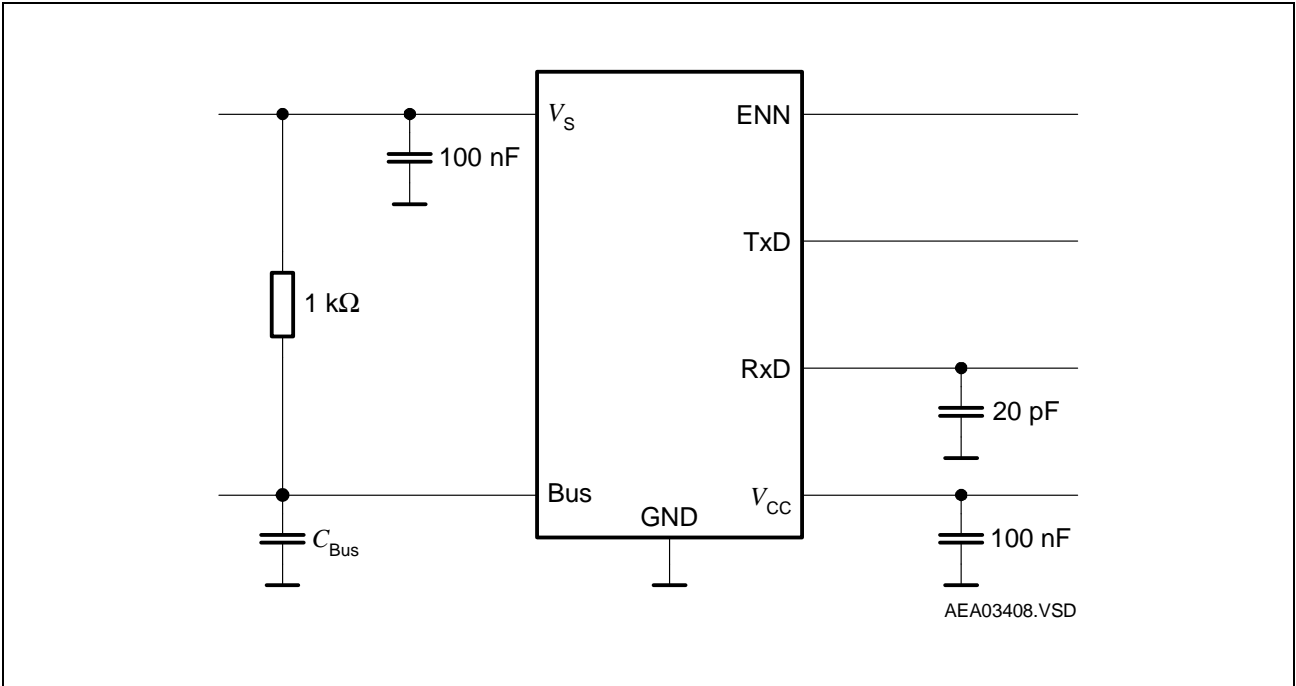
Parameter	Symbol	Limit Values			Unit	Remark
		Min.	Typ.	Max.		
<b>Dynamic Transceiver Characteristics</b>						
Falling edge slew rate	S <sub>bus(L)</sub>	-3	-2.0	-1	V/μs	<sup>1)</sup> 60% > V <sub>bus</sub> > 40% 1 μs < (τ = R <sub>L</sub> × C <sub>BUS</sub> ) < 5 μs; V <sub>CC</sub> = 5 V; V <sub>S</sub> = 13.5 V
Rising edge slew rate	S <sub>bus(H)</sub>	1	1.5	3	V/μs	<sup>1)</sup> 40% < V <sub>bus</sub> < 60% 1 μs < (τ = R <sub>L</sub> × C <sub>BUS</sub> ) < 5 μs; V <sub>CC</sub> = 5 V; V <sub>S</sub> = 13.5 V
Slope symmetry	t <sub>slopesym</sub>	5		-5	μs	t <sub>fslope</sub> - t <sub>rslope</sub> V <sub>S</sub> = 18 V
Propagation delay TxD LOW to bus	t <sub>d(L),T</sub>	–	1	3	μs	V <sub>CC</sub> = 5 V
Propagation delay TxD HIGH to bus	t <sub>d(H),T</sub>	–	1	3	μs	V <sub>CC</sub> = 5 V
Propagation delay bus dominant to RxD LOW	t <sub>d(L),R</sub>	–	1	6	μs	V <sub>CC</sub> = 5 V; C <sub>RxD</sub> = 20 pF
Propagation delay bus recessive to RxD HIGH	t <sub>d(H),R</sub>	–	1	6	μs	V <sub>CC</sub> = 5 V; C <sub>RxD</sub> = 20 pF
Receiver delay symmetry	t <sub>sym,R</sub>	-2	–	2	μs	t <sub>sym,R</sub> = t <sub>d(L),R</sub> - t <sub>d(H),R</sub>
Transmitter delay symmetry	t <sub>sym,T</sub>	-2	–	2	μs	t <sub>sym,T</sub> = t <sub>d(L),T</sub> - t <sub>d(H),T</sub>
Duty cycle D1	t <sub>duty1</sub>	0.396	–	–	μs	duty cycle <sup>1)</sup> TH <sub>Rec</sub> (max) = 0.744 × V <sub>S</sub> ; TH <sub>Dom</sub> (max) = 0.581 × V <sub>S</sub> ; V <sub>S</sub> = 7.0 ... 18 V; t <sub>bit</sub> = 50 μs; D1 = t <sub>bus_rec(min)}/2 t<sub>bit</sub>;</sub>
Duty cycle D2	t <sub>duty2</sub>	–	–	0.581	μs	duty cycle <sup>2)</sup> TH <sub>Rec</sub> (max) = 0.422 × V <sub>S</sub> ; TH <sub>Dom</sub> (max) = 0.264 × V <sub>S</sub> V <sub>S</sub> = 7.6 ... 18 V; t <sub>bit</sub> = 50 μs; D2 = t <sub>bus_rec(max)}/2 t<sub>bit</sub>;</sub>

**Table 4 Electrical Characteristics (cont'd)**

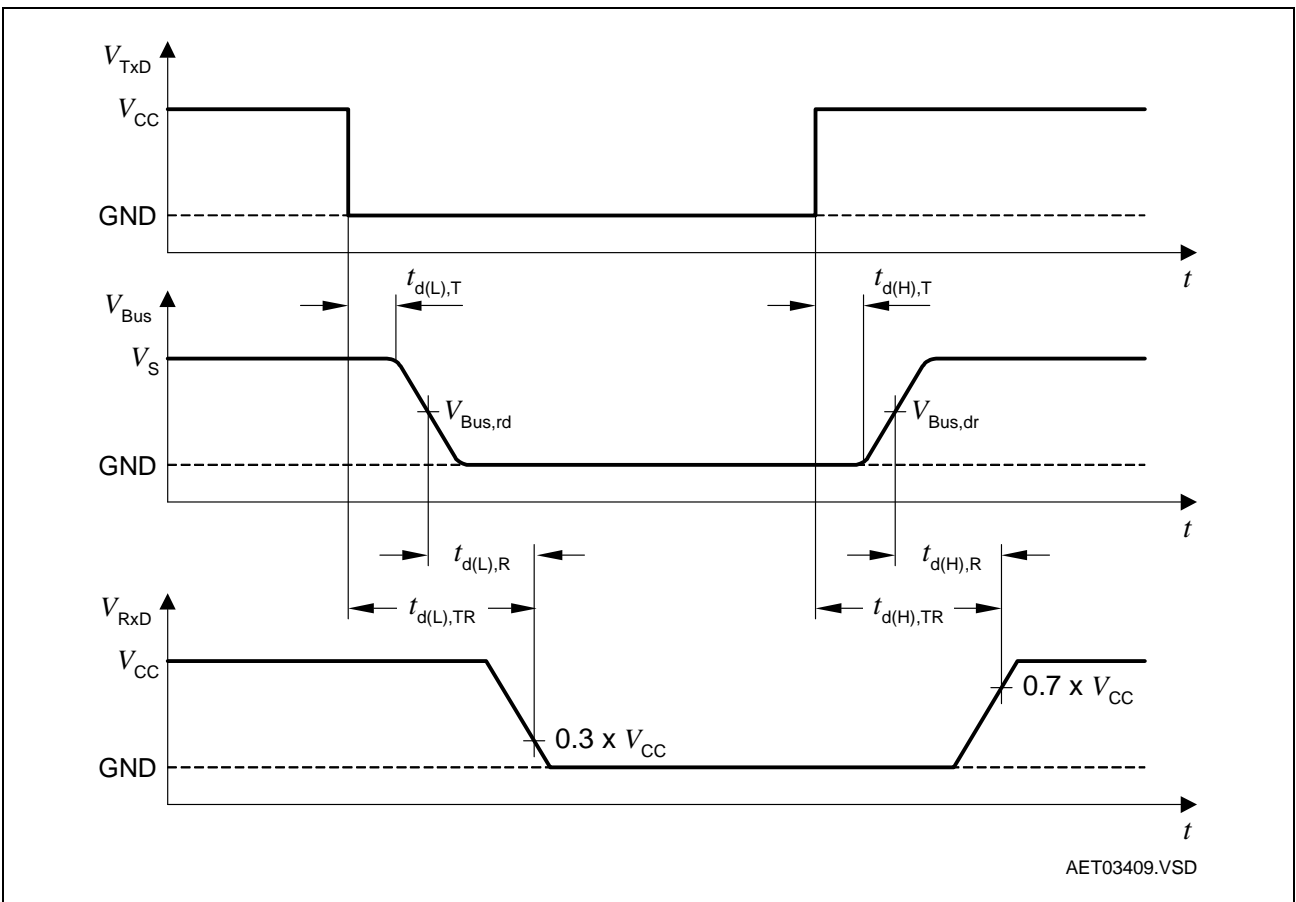
4.5 V < V<sub>CC</sub> < 5.5 V; 6.0 V < V<sub>S</sub> < 27 V; R<sub>L</sub> = 500 Ω; V<sub>ENN</sub> < V<sub>ENN,ON</sub>; -40 °C < T<sub>j</sub> < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Remark
		Min.	Typ.	Max.		
Wake-up delay time	t <sub>wake</sub>	30	100	150	μs	T <sub>j</sub> < 125 °C
				170	μs	T <sub>j</sub> < 150 °C
Delay time for mode change	t <sub>snorm</sub>			50	μs	

1) Bus load conditions concerning LIN spec 2.0 C<sub>bus</sub>, R<sub>bus</sub> = 1 nF, 1 kΩ / 6.8 nF, 660 Ω / 10 nF, 500 Ω



**Figure 4 Test Circuits**



**Figure 5 Timing Diagram for Dynamic Characteristics**

Application

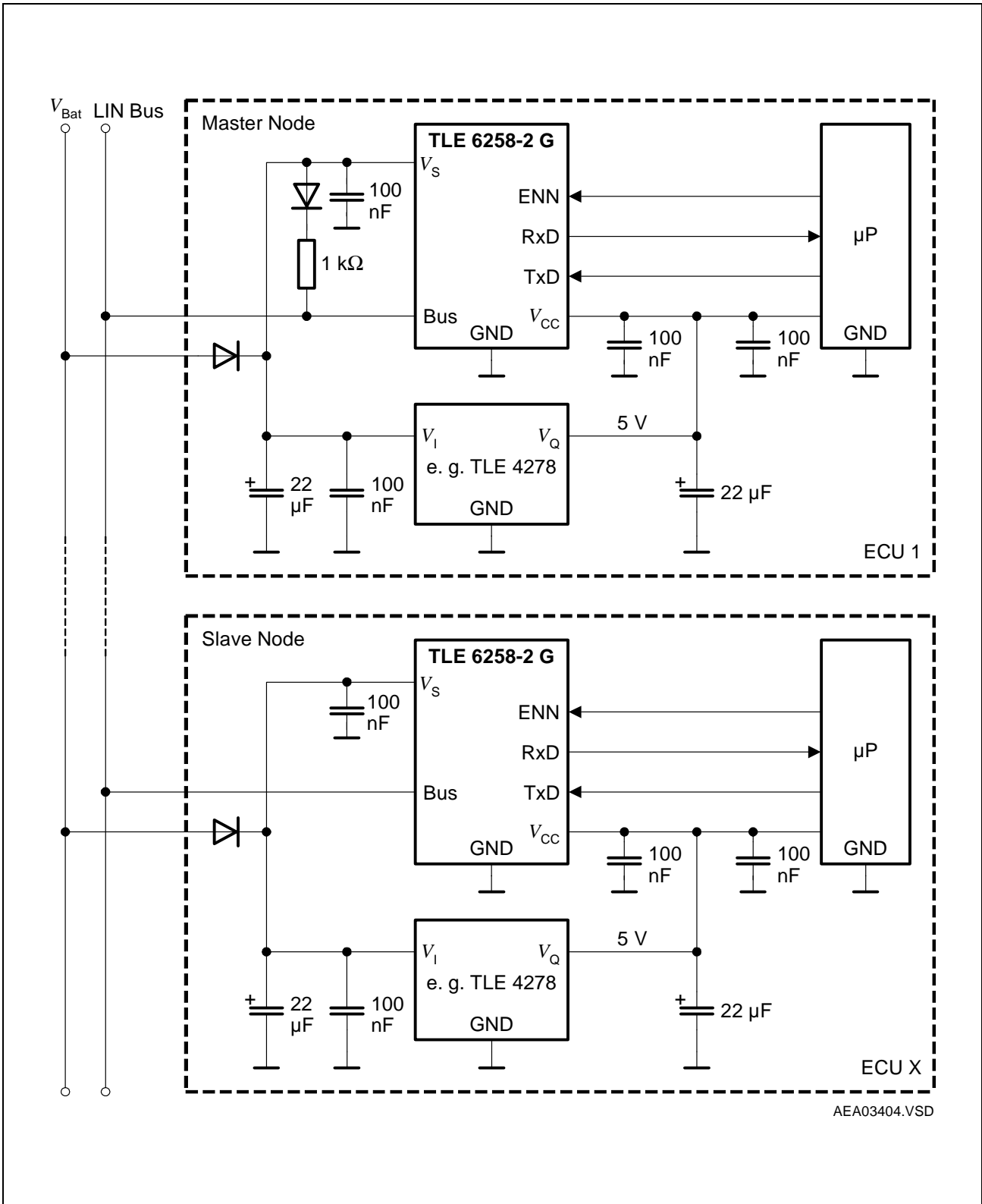


Figure 6 Application Circuit

Package Outlines

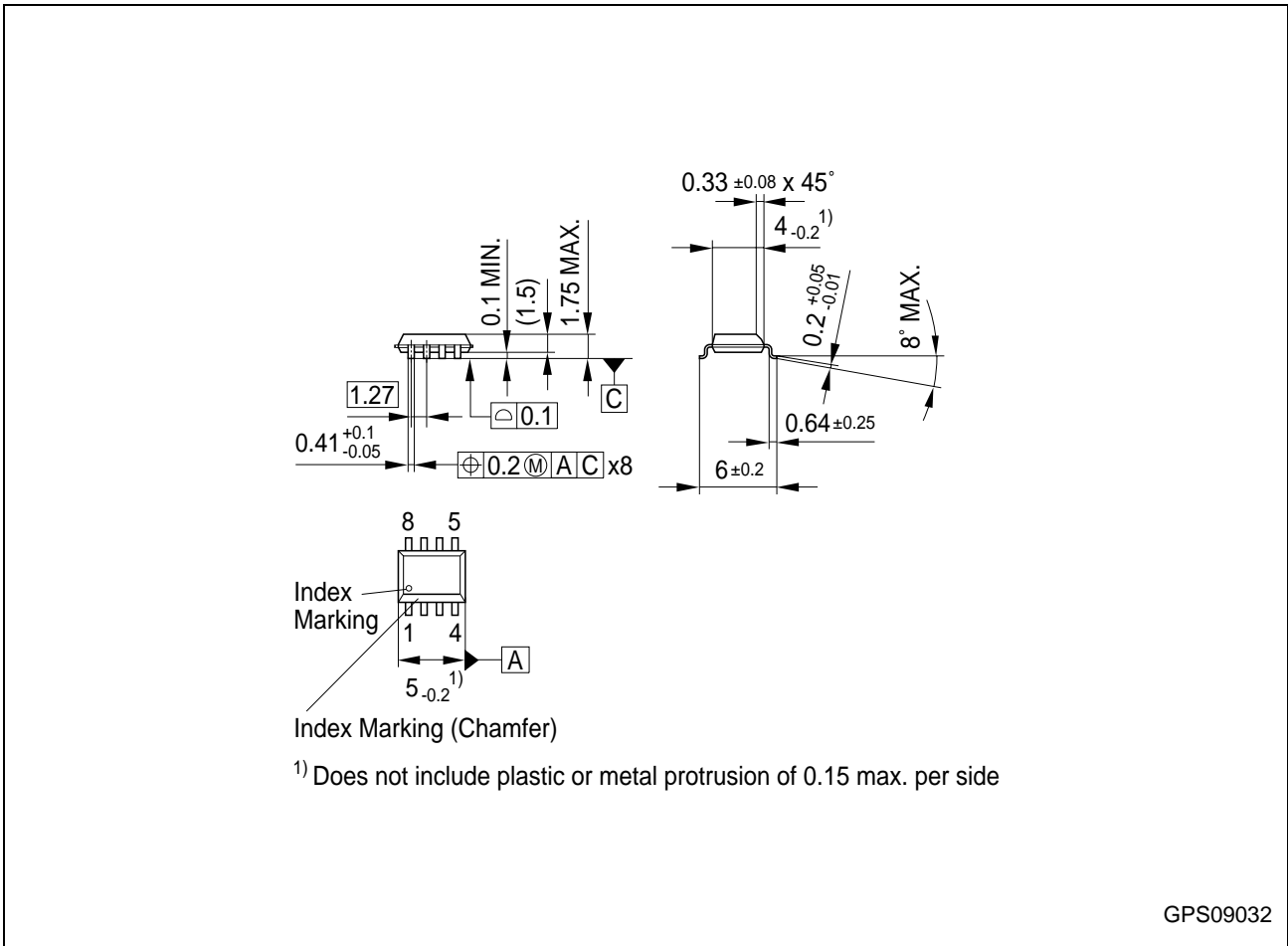


Figure 7 P-DSO-8-3 (Plastic Dual Small Outline)

You can find all of our packages, sorts of packing and others in our Infineon Internet Page "Products": <http://www.infineon.com/products>.

SMD = Surface Mounted Device

Dimensions in mm